

ArchES Computing Systems



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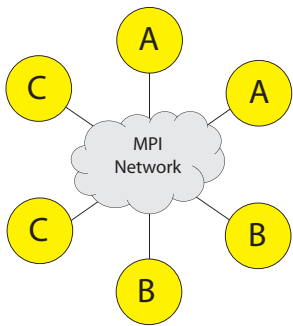
Uniting CPUs and FPGAs through MPI

High Performance Reconfigurable Computing (HPRC) combines the power of conventional microprocessors with the speed and configurability of Field Programmable Gate Arrays.

ArchES Computing Systems Corp. provides the infrastructure and the expertise to harness the power of HPRC machines such as the Nallatech FSB FPGA Accelerator Platform.

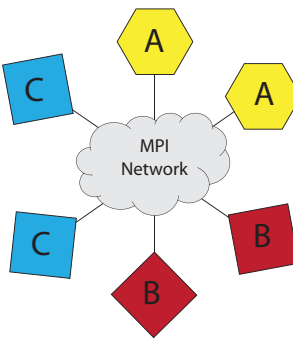
Configurability

Application Development View using Standard MPI



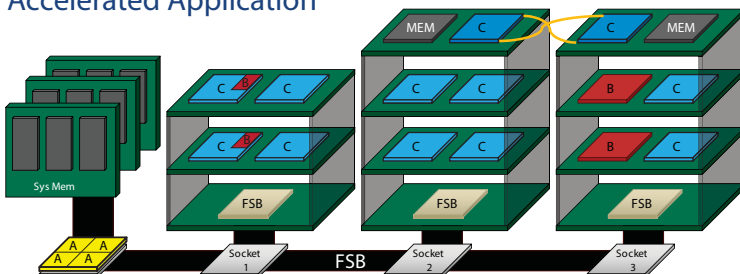
- Build, test, debug application
- Optimize algorithms
- Parallelize on standard HPC
- Identify heavy CPU processes

Mapping to Heterogeneous Processing Elements



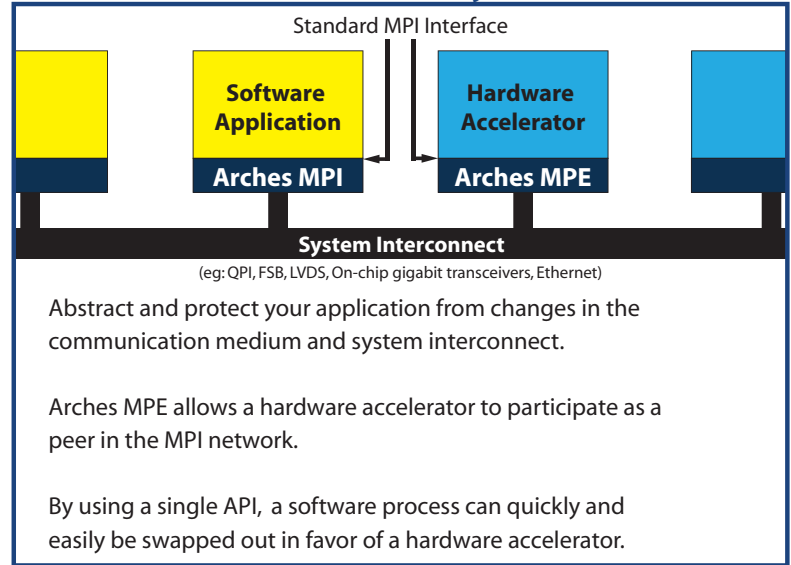
- Offload CPU intensive components to dedicated hardware accelerators
 - Remaining components can target x86 CPU or embedded processors
 - Simplify the programming model by using a single API: MPI
- x86 CPU
 - Hardware Accelerator
 - Embedded Processor

Accelerated Application

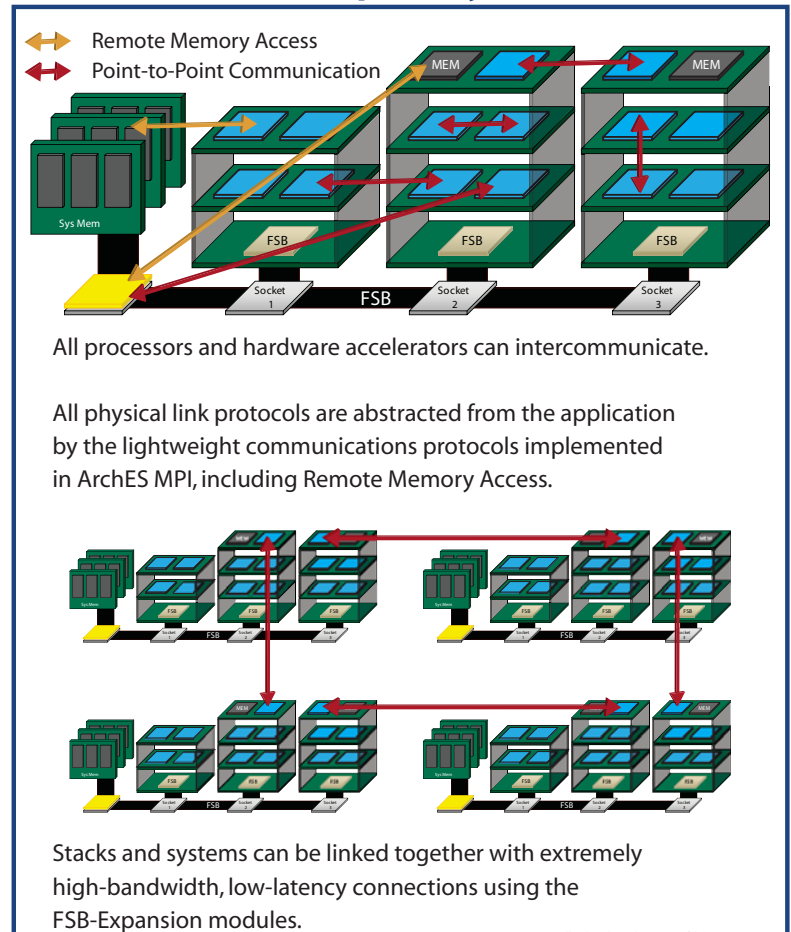


Application accelerated through dedicated hardware accelerators and CPUs interconnected throughout system.

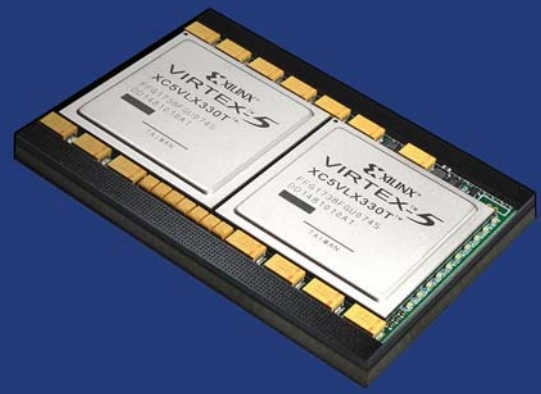
Portability



Capability



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Products and Services

Arches-MPI

Arches-MPI is an MPI implementation that enables high-performance communication between all CPU-based processes and FPGA-based hardware engines.

Arches-MPI enables an application to be written in C or C++ and then quickly ported to a hardware/software hybrid system. Parallel processes can synchronize and communicate transparently regardless of whether they are implemented as a software process or a hardware engine. On systems such as the Nallatech FSB Platform, Arches-MPI takes advantage of the tight coupling of the Nallatech FSB-FPGA modules to system processors.

The Arches-MPI suite is an MPI implementation consisting of a software MPI library and small communication blocks implemented on the FPGA fabric. These Message Passing Engines (Arches-MPE) allow user-defined hardware engines and embedded processors to participate in an MPI network. In this way a message can be sent to a hardware engine, an embedded processor, or a CPU using standard MPI functions, reducing overall complexity and learning curves.

The Arches-MPI network provides a routing mechanism to relay point-to-point messages between any two computing elements regardless of their physical location. Endpoints can be any combination of hardware or software, on the same FPGA, in different FPGAs, between a CPU and an FPGA, or even between different systems. Since the communication interface between individual processes is standard MPI, many applications require minimal intervention in the porting process between different machine vendors or across new generations of FPGAs.

Advanced Computing Platform Development Kit

The ACP Development Platform is a development kit for quickly realizing the power of embedded processing. It combines the Nallatech FSB Platform with an Arches-MPI development kit.

Complete System Design Service

Arches Computing Systems can provide a complete system design service to get your application up and running in a heterogeneous CPU/FPGA environment.

With in-house software and digital hardware developers who created the entire Arches-MPI suite, as well as an extensive development relationship with Xilinx Inc. to enable Arches-MPI on the Nallatech FSB Platform, Arches Computing Systems is in an excellent position to assist you with your design needs.

We are able to assist you in any phase of the development cycle. From algorithm partitioning, to software and hardware implementation, we have the expertise to ensure your success.

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